Sun Yat-sen University College Student Innovation Training Project

application

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| Item Number | 1 | | |
| project name | Cost-effective experimental digital control system | | |
| Project manager | Xu Wanyou | contact number | 13550841943 |
| College | Physics and Astronomycollege | | |
| student ID | 2234160 | professional class | Physics 22Class 3 |
| mentor | ThibaultThomasVogt | | |
| Email | ttvogt@mail.sysu.edu.cn | | |
| Date of Application | Automatic acquisition | | |

Sun Yat-sen University Academic Affairs Department

#### 1. Basic situation

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| project name | | Cost-effective experimental digital control system | | | | | | | |
| Discipline | | First-level subject categories:physics Subject level two:Atomic and Molecular Physics | | | | | | | |
| project source | | □ A. Students choose topics independently, which comes from their long-term accumulation and interest in the topic.  ☑B. From the topic selection of teachers’ scientific research projects  □ C. Students are responsible for selecting topics for projects entrusted by society and enterprises. | | | | | | | |
| Application Amount | | 23700.00 yuan | Project deadline | One year | Project level to be applied for | | | nationclass | |
| principal | | Xu Wanyou | gender | female | nationality | | Han nationality | Date of birth | 2003Year9moon |
| student ID | | 22344160 | contact number | Mobile: 13550841943 | | | | | |
| mentor | | ThibaultThomasVogt | contact number | cell phone:13322866303 | | | | | |
| Project Description | | This project aims to design a cost-effective real-time (delay within ms) digital monitoring and control system that can be widely used in physical experiment terminals. This system will serve the collection-operation-feedback output process of experimental platform data based on digital signals such as TTL and analog signals. The specific implementation routes of the system are diverse, and the overall idea is: one core, multiple terminals. We expect that this can effectively handle large amounts of calculations, large data flows, and provide integrated control of the experimental platform. | | | | | | | |
| The person in charge’s previous participation in scientific research | | none | | | | | | | |
| Instructing teachers to undertake scientific research projects | | The magneto-optical trap system serves to capture a single cesium atom and provides platform monitoring and control services for the mentor's bit gate construction of Rydberg ion detection and neutral atom calculations. | | | | | | | |
| Instructor’s support for this project | | Teachers will provide some basic components and equipment and power control systems and provide a dedicated optical experiment platform for system construction. | | | | | | | |
| Main members of the project team | Name | student ID | | college | professional class | contact number | | Project division of labor | |
| Lu Boyu | 21305203 | | School of Physics and Astronomy | Physics Class 1 | 15087364733 | | Mainly responsible for the overall design of FPGA system and the overall design, packaging and manufacturing. | |
| Chen Zhengyuan | 21305342 | | School of Physics and Astronomy | Physics Class 3 | 13534025498 | | Mainly responsible for overall software design and computing framework development planning. | |
| Jia Haoran | 22344071 | | School of Physics and Astronomy | Physics Class 3 | 13548082165 | | Mainly responsible for ADC\DAC synchronous communication design, PC-side GPU system design, and CUDA programming development. | |
| Pan Jiarui | 22344112 | | School of Physics and Astronomy | Physics Class 2 | 13430812188 | | Mainly responsible for RTOS system development, PC-side GPU system design, and CUDA programming development. | |
| Xu Wanyou | 22344160 | | School of Physics and Astronomy | Physics Class 3 | 13550841943 | | Mainly responsible for CUDA programming and HDL programming development. | |
| mentor | Name | Job number | | College/Unit | job title | contact number | | e-mail | |
| ThibaultThomasVogt | 190327 | | School of Physics and Astronomy | Associate Professor | 13322866303 | | ttvogt@mail.sysu.edu.cn | |

#### 2. Basis for project establishment (can add pages)

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| **1. Research purpose**  Independently develop and implement a cost-effective pan-terminal information collection, highly parallel computing and processing, and multi-channel controllable outputlaboratoryUniversal digital intelligent system. This replaces a large number of expensive non-domestic scattered low-digital, low-intelligent experimental measurement units, processing units, and display units in the laboratory.  It is expected to achieve comprehensive centralized monitoring and control of the experimental platform in a high-speed and high-density environment.  **2. Research content**  This project will cooperate with Mr. Thibault’s 2024The development of other projects under the Daiso Group aims to replace the scattered monitoring and control units in these projects, and establish reasonable high and low speed channels to adapt to devices that require different levels of monitoring and control. Therefore, the system will be researched and designed in the following steps:  (1) Exploration and hardware implementation of algorithms for converting high- and low-speed hybrid digital parallel signals into serial signals.  (2) Explore the real-time processing and output of signals by PC based on RTOS.  (3) Exploration of highly parallel and high-speed data processing algorithms based on matrix convolution (vectorization).  (4) Integrated implementation of FPGA (Field Programmable Gate Array) dedicated circuits.  (5) High and low speed (Analog+Data) dual-channel decoupled output signals.  wps  Overall flow chart  **3. Research status and development trends at home and abroad**  With the rapid development of science and technology, the signals that need to be monitored and controlled in experimental systems show a trend of large number, variety, high coupling, and high real-time requirements. In the past, the mixed transmission and processing of analog signals and digital signals has become more and more problematic. Significantly. In domestic experimental systems, due to diverse measurement requirements and the compatibility of different equipment, there is often confusion in the transmission and processing of analog and digital signals. These phenomena often lead to problems such as unsatisfactory experimental efficiency and reduced experimental accuracy.  A universal digital experiment monitoring and control system can improve experimental efficiency and accuracy, allowing experimenters to focus more on experiments rather than being burdened with complicated experimental data collection and processing work. In the digital/computer field, good encapsulation of each layer of the system allows developers to get twice the result with half the effort, which is the cornerstone of the rapid development of the entire digital/computer field. Therefore, a large number of proven successful models in the digital/computer field can be used as a reference when building a general digital experimental monitoring and control system.  This project hopes to use the achievements made in the digital/computer field to build a universal digital experimental monitoring and control system to solve the above-mentioned problems that plague some physics experimenters and help the development of the field of physical experiments.  **4. Innovation points and project features**  **Innovation:**  (1) The benefits of converting analog signals into digital signals for transportation and processing are: the problem of signal attenuation is not serious during digital signal transmission; errors only occur during mutual conversion, so it can be easily controlled by simply controlling the errors at the source. Good error; digital signals are processed using chips with powerful computing power, with high throughput and fast response.  (2) After the different channel data generated in the laboratory are synchronized in time, the output of each channel in a certain frame is often calculated comprehensively from the data of each channel in the previous frame, and there is no time dependence on the data output of each channel under this algorithm. Collecting data from each channel and then applying vectorization/highly parallel processing methods (mainly matrix convolution) is suitable for high-speed parallel processing of large amounts of data with the above characteristics.  (3) In order to cope with various experimental scenarios, digital experimental monitoring and control systems are required to be designed to be universal; however, often in specific experimental scenarios, digital experimental monitoring and control systems using dedicated circuits can also be competent at the task, and dedicated circuits save computing power and resource. FPGA is designed to be circuit programmable, so that different special circuits can be programmed for different experiments on one chip. At the same time, FPGA also has the ability to program general computing circuits. Therefore, a digital experimental monitoring and control system that relies on FPGA chips for data processing has the same monitoring and control capabilities as a system that relies on general-purpose computing circuits (when the computing power of FPGA and GPU is equivalent), and saves more computing power and resources.  (4) For experimental sites that are only suitable for PCs, we also provide solutions based on RTOS transmission and real-time processing of large amounts of multi-channel data.  **Program features:**  Through the digitization and centralization of laboratory data, the data processing capabilities of digital computing chips can be fully utilized according to the characteristics of laboratory data, while achieving more refined, automated control and more humane interactive functions.  **5. Technical route, problems to be solved and expected results**  **Technical route:**  This project will rely on high- and low-speed ADCs from pan-terminals to complete digital signal collection, and establish reasonable high- and low-speed channels to adapt to devices that require different levels of monitoring and control. For high-speed devices m (≈200), it is expected to achieve ms-level response control, and the high-speed ADC frequency of the pan-terminal is at least 20MHz, digital signal line transmission rate is at least m\*20KB/s(≈4MB/s); for low-speed devices n (≈100), it is expected to achieve S-level response control, and the low-speed ADC frequency of the pan-terminal is at least 20KHz, digital signal line transmission rate is at least n\*20B/s(≈2KB/s).  Since there are a large number of analog-to-digital conversions and parallel-to-serial conversions, as well as the need to separate high- and low-speed channels, there is a data alignment problem, which requires the development of a universal and powerful synchronization mechanism to solve this problem.  High-speed digital signal data places high demands on real-time computing performance. Assume that the parallelism of the computing system used is h (generally>m), the running frequency is q (for GPU≈500, for FPGA≈100)MHz, it is required to be within 1000\*q\*h/m(at 105Magnitude) cycle to complete the calculation. It seems abundant, but in fact it requires the development of good I/OWork with caching strategies to avoid these cycles being wasted waiting for data to be loaded due to cache misses and other issues.  **To solve the problem**:  (1) Converting high- and low-speed hybrid digital parallel signals to serial signals and high- and low-speed (Analog+Data) dual-channel decoupled output signals require complex synchronization mechanisms built on synchronization signals.  (2) Digital signals need to be used in conjunction with the protocol. In order to meet system requirements (RTOS+GPU, FPGA) may need to adopt different protocols or modify existing protocols or independently design protocols to ensure protocol consistency.  (3) FPGA development spans the electrical and logic fields, and development is difficult.  (4) requires additional debugging in the PC or FPGA system to make targeted I/OOand caching strategies to meet performance requirements.  **Expected results**:  Basic results: Establishing reasonable high- and low-speed channels for differentiated monitoring and control of different devices, using RTOS+Complete the implementation of highly parallel data processing algorithms under the GPU system.  Ideal result: Realize 2 functions under the name of Mr. Thibault under the FPGA system024Comprehensive, automated, and more refined monitoring and control of instruments in laser projects developed under the Daiso Group.  Expansion results: Graphical interface interaction is realized through the designed visual interaction interface and external GUI program.  **6.Project research progress arrangement**  January to March 2024: Literature study (preliminary study of the computing principles required for this project), forming basic digital awareness, supplementing electronic technology knowledge, and learning to use Git as a work information terminal.  Early March to the end of March 2024: Be familiar with the modules of the host system.  Early April to the end of April 2024: Assemble the host system as a whole and start testing the CPU system.  Early May to the end of July 2024: Programming and debugging of GPU (CUDA) computing system under RTOS.  Early August to the end of September 2024: Programming and debugging of FPGA (HDL) computing system.  Early October to the end of November 2024: Establishment of system hardware packaging and GUI and other external human-computer interaction systems.  Early December to mid-December 2024: Prepare for completion.  **7. Already have a foundation**  **(1) Research accumulation and achievements related to this project**  Some of the team members have participated in Daiichi 23 and used the MCU system to partially realize the expected functions of this project.  In terms of software programming, some students have participated in computing-related scientific research training such as mathematical simulation competitions and automated image recognition projects. For example, they have experience in processing very large sparse matrices, iterative convergence algorithms, internal and external linking algorithms, local compilation, and vectorized matrix convolution algorithms. , automated graphics programming, and a series of studies on proving geometric optimal problems in three-dimensional space.  In terms of hardware design, some team members have experience in independently designing the internal PCB structure of a small unit system and realizing the overall package structure or disassembling and assembling the PC side of a large structure. They have certain experience in heat dissipation system design, circuit design, and shell design.  **(2) Conditions that are already in place, conditions that are still lacking and solutions**  Most members of the project already have experience inEngineering Drawing and CAD,Calculation method, computational physics, structured and object-oriented programming (C language), electronic technology theory and experiment and other basic related skills mastered in a series of courses.  The knowledge accumulated by some team members has a relatively comprehensive coverage of computer systems, a preliminary understanding of computer I/O, CPU architecture, bus system, operating system kernel, Git (distributed file system), and AT&T Assembly, C/C++,MATLAB, PowerShell, Python, Wolfram, Haskell, Scheme, LabVIEW and other programming languages ​​have a preliminary grasp.  In summary, this group is fully equipped to further learn RTOS and GPU programming (OpenCL/CUDA), FPGA programming (Verilog/CHISEL), GUI (WinForms/WPF) system capabilities and foundation.  The main difficulty lies in the large gap in computer understanding between team members and the huge workload.  The current solution is to assign clear learning goals (pointing to a mutually unknown independent field) to group members with weak foundations from the beginning of the topic to share the overall pressure. |

#### 3. Budget

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| **Expenditure account** | **Budget funds (yuan)** | **The main purpose** | **Funding plan released in stages (yuan)** | |
| **first half stage** | **second half stage** |
| Total budget funds | 23700.00 |  | 11850.00 | 11850.00 |
| 1. Business expenses | 7300.00 |  | 3650.00 | 3650.00 |
| (1) Hardware cloud service fee | 1500.00 | Cloud simulation of hardware | 750.00 | 750.00 |
| (2) Software cloud service fee | 1500.00 | Cloud testing of software | 750.00 | 750.00 |
| (3) Expert consultation fees | 1500.00 | Seek technical consultation for a fee when necessary | 750.00 | 750.00 |
| (4) Meeting and travel expenses | 600.00 | Weekly group meeting of five people | 300.00 | 300.00 |
| (5) Literature search fee | 1200.00 | To get the reference code, purchase a membership to the relevant web development forum | 600.00 | 600.00 |
| (6) Paper publication fee/Patent application fee | 1000.00 | Patent application may be considered | 500.00 | 500.00 |
| 2. Instrument and equipment purchase fees | 2000.00 | Supplementary test signal generator | 1000.00 | 1000.00 |
| 3. Experimental device trial production fee | 1800.00 | Experimental device processing and packaging | 900.00 | 900.00 |
| (1) Manufacturing of computing host casing | 600.00 | Protect vulnerable electronic systems | 300.00 | 300.00 |
| (2) Construction of computing host cooling system | 600.00 | Fixed points to cool down hot components for normal operation | 300.00 | 300.00 |
| (3) Computer power supply production | 600.00 | Power your PC | 300.00 | 300.00 |
| 4. Material fee | 12600.00 | Purchase of GPU chips, FPGA development boards, and peripheral equipment | 6300.00 | 6300.00 |
| (1)GPU chip purchase | 3000.00 | With high-speed GPU chip (expected model is GTX1660S) Perform parallel operations | 1500.00 | 1500.00 |
| (2)PC peripherals purchase | 1200.00 | Provide hardware foundation for human-computer interaction such as GUI design | 600.00 | 600.00 |
| (3) FPGA chip and development board purchase | 6000.00 | FPGA chips are used to program professional circuits | 3000.00 | 3000.00 |
| (4) FPGA supporting peripherals | 1200.00 | Provide the hardware foundation for human-computer interaction for FPGA systems | 600.00 | 600.00 |
| (5) High-speed mid-range signal RF communication cable purchase | 900.00 | Connect the computing host and input and output terminals to transmit high-speed analog signals | 450.00 | 450.00 |
| (6) High-speed digital data cable purchase | 300.00 | Connect the computing host and input and output terminals to transmit high-speed digital signals | 150.00 | 150.00 |
| Total budget funds | 23700.00 |  | 11850.00 | 11850.00 |

#### 4. Opinions of instructors

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| **tutor:\*\*\***  **Yearmoonday** |

#### 5. Recommendations from departments

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| **Seal:**  **Yearmoonday** |